Appendix C

31 28	27 26	25	24 21	20	19 16	15 12	11 0
Cond	00	I	OpCode	S	Rn	Rd	Operand 2

Cond: Condition field		**OpCode:** Operation code	
0000	EQ (EQual)	0000	AND
0001	NE (NEver)	0001	EOR
0010	CS (Carry Set)	0010	SUB
0011	CC (Carry Clear)	0011	RSB
0100	MI (MInus)	0100	ADD
0101	PL (PLus)	0101	ADC
0110	VS (oVerflow Set)	0110	SBC
0111	VC (oVerflow Clear)	0111	RSC
1000	HI (HIgher)	1000	TST
1001	LS (Lower or Same)	1001	TEQ
1010	GE (Greater or Equal)	1010	CMP
1011	LT (Less Than)	1011	CMN
1100	GT (Greater Than)	1100	ORR
1101	LE (Less than or Equal)	1101	MOV
1110	AL (ALways)	1110	BIC
1111	NV (NeVer)	1111	MVN

Instruction set

Data Processing

I: Immediate operand bit. This defines exactly what Operand 2 is. If the I bit is 0, Operand 2 is a register, with the register number held in bits 0 to 3 and the shift applied to that register in bits 4 to 11. If the I bit is 1, Operand 2 is an immediate value, with bits 0 to 7 holding the 8 bit value, and bits 8 to 11 holding the shift

31 28	27 25	24	23 0
Cond	101	L	Offset

applied to that value.

S: Set condition codes. If this bit is set to 0, the condition codes are not altered after the instruction has

31 28	27 22	21	20	19 16	15 12	11 8	7 4	3 0
Cond	000000	A	S	Rn	Rd	Rs	1001	Rm

executed. If it is set to 1, they are altered.

Rn: First operand register.

Rd: Destination register.

31 28	27 26	25	24	23	22	21	20	19 16	15 12	11 0
Cond	01	I	P	U	B	W	L	Rn	Rd	Offset

Branch and Branch with link

L: Link bit. 0=Branch, 1=Branch with link

Multiply and multiply-accumulate

A: Accumulate bit. 0=multiply, 1=multiply with accumulate

31 28	27 25	24	23	22	21	20	19 16	15 0
Cond	100	P	U	S	W	L	Rn	Register list

Single Data transfer

P: Pre/Post indexing. 0=post (offset added after transfer). 1=pre (offset added before transfer).

31 28	27 24	23 0
Cond	1111	Comment field (ignored by ARM)

U: Up/Down bit. 0=down (Offset subtracted from base). 1=Up (Offset added to base).
B: Byte/Word bit. 0=transfer word, 1=transfer byte.

31 28	27 24	23 20	19 16	15 12	11 8	7 5	4	3 0
Cond	1110	CP Opc	CRn	CRd	CP#	CP	0	CRm

W: Write-back. 0=No write back, 1=Write address into base.

Block data transfer

31 28	27 25	24	23	22	21	20	19 16	15 12	11 8	7 0
Cond	110	P	U	N	W	L	Rn	CRd	CP#	Offset

S: PSR & Force user mode. 0=do not load PSR or force user mode. 1=load PSR or force user mode.

Software Interrupt

31 28	27 24	23 21	20	19 16	15 12	11 8	7 5	4	3 0
Cond	1110	CP Opc	L	CRn	Rd	CP#	CP	1	CRm

Co-processor data operations

CP Opc: Co-processor operation code. **CRn:** Co-processor operand register. **CRd:** Co-processor

31 28	27 24	23 8	7 4	3 0
Cond	0001	xxxxxxxxxxxxxxxx	1xx1	xxxx

31 28	27 25	24 5	4	3 0
Cond	011	xxxxxxxxxxxxxxxxxxxx	1	xxxx

destination register. **CP#:** Co-processor number. **CP:** Co-processor information

Co-processor data transfers

Co-processor register transfers

L: Load/Store bit. 0=Store to co-processor, 1=Load from co-processor.

Undefined instructions.